AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Previously presented) A method comprising:
receiving a calibration clock over a terminal;
generating at least one control value in a control loop to lock a clock generated by a controllable oscillator to a multiple of the calibration clock; and
storing a value corresponding to the at least one control value in a non volatile memory.

2. (Original) The method as recited in claim 1 wherein the control loop is a phase-locked loop.

3. (Previously presented) The method as recited in claim 2 further comprising generating at least a second control value using the phase-locked loop to lock the clock generated by the controllable oscillator to a multiple of the calibration clock and wherein the at least one control value and the second control value are generated at first and second temperatures.

4. (Original) The method as recited in claim 3 further comprising storing the first and second temperatures in the non-volatile memory.

5. (Previously presented) The method as recited in claim 3 further comprising storing a difference between the at least one control value at the first temperature and the second control value at the second temperature.

6. (Previously presented) The method as recited in claim 2 further comprising determining if the phase-locked loop is locked to the calibration clock during receipt of the calibration clock.

7. (Original) The method as recited in claim 1 wherein the multiple is one of an integer multiple and fractional multiple of the calibration clock.

8. (Canceled)

9. (Canceled)

10. (Currently amended) The method as recited in claim 1 further comprising supplying a fixed frequency reference from a fixed frequency reference source to synthesize the ~~output~~ clock.

11. (Original) The method as recited in claim 10 wherein the fixed frequency reference source is one of a crystal and a surface acoustic wave (SAW) device.

12. (Original) The method as recited in claim 10 further comprising receiving the calibration clock while the nonvolatile memory, fixed frequency reference source and the phase-locked loop are in a sealed package.

13. (Original) The method as recited in claim 1 further comprising receiving at least one command sequence over the terminal prior to receiving the calibration clock.

14. (Original) The method as recited in claim 13 wherein the at least one command sequence programs a storage location and determines a divider value utilized by a divider circuit in the phase-locked loop according to a value in the storage location.

15. (Original) The method as recited in claim 13 wherein the terminal is bidirectional and a serial command received over the terminal is a read command causing data to be provided on the terminal.

16. (Original) The method as recited in claim 2 further comprising selectively coupling the controllable oscillator to a feedback path to form the phase-locked loop.

17. (Original) The method as recited in claim 1 wherein the controllable oscillator is supplied a digital control value.

18. (Original) The method as recited in claim 1 further comprising setting a voltage control input to midrange prior to providing the calibration clock.

19. (Original) The method as recited in claim 1 further comprising disabling a voltage controlled crystal oscillator (VCXO) mode of operation prior to providing the calibration clock.

20. (Original) The method as recited in claim 1 further comprising disabling a temperature compensation mode of operation prior to providing the calibration clock.

21. (Previously presented) A method of calibrating a device that includes a controllable oscillator and a resonating device that supplies a fixed reference frequency used by the controllable oscillator to synthesize an output clock, the controllable oscillator and the resonating device being mounted in a package, the method comprising:

supplying a calibration clock to an input/output terminal of the device;

generating a control value in a control loop of the device to cause the controllable oscillator to lock to a multiple of the calibration clock; and

storing a value determined according to the control value in a non-volatile memory in the device.

22. (Previously presented) The method as recited in claim 21 wherein a phase-locked loop is selectively implemented as the control loop and includes the controllable oscillator and generates the control value during calibration.

23. (Original) The method as recited in claim 21 wherein the resonating device is one of a crystal and a surface acoustic wave (SAW) device.

24. (Original) The method as recited in claim 21 further comprising receiving at least one command sequence over the input/output terminal prior to receiving the calibration clock.

25. (Original) The method as recited in claim 24 wherein the at least one command sequence determines a divider value utilized by a divider circuit in a phase-locked loop generating the control value during calibration, the divider value being determined according to a value in the storage location.

26. (Previously presented) An apparatus comprising:

a controllable oscillator coupled to receive a reference frequency and a control value and to output a clock signal;

a terminal for receiving a calibration clock signal;

a phase-locked loop circuit including the controllable oscillator is coupled to receive the calibration clock signal and generate a correction factor to cause the controllable oscillator to lock to a multiple of the calibration clock signal ; and

a non-volatile memory storing a value corresponding to the correction factor.

27. (Original) The apparatus as recited in claim 26 wherein the controllable oscillator is selectively coupled as part of the phase-locked loop.

28. (Previously presented) The apparatus as recited in claim 26 further comprising memory locations storing a history of correction factors determined during calibration of the apparatus.

29. (Original) The apparatus as recited in claim 26, wherein the apparatus is further coupled to respond to input signals on the terminal as serial commands.

30. (Original) The apparatus as recited in claim 26 wherein the apparatus is an integrated circuit.

31. (Original) The apparatus as recited in claim 26 wherein the terminal is a pin on a package holding a semiconductor device.

32. (Original) The apparatus as recited in claim 26 wherein the terminal is bi-directional.

33. (Original) The apparatus as recited in claim 26, further comprising an integrated circuit including a control circuit coupled to determine when the terminal has had a particular value for longer than a predetermined time period, and to supply an internal output enable signal having the particular value to selectively enable the one or more clock signals according to the particular value.

34. (Original) The apparatus as recited in claim 33 wherein transitions on the terminal that occur in less than the predetermined time period are determined to be serial data communication signals.

35. (Original) The apparatus as recited in claim 26, further comprising an integrated circuit including the controllable oscillator and the phase-locked loop.

36. (Original) The apparatus as recited in claim 35 wherein the apparatus includes a resonating device supplying the reference frequency and a package holding the resonating device and the integrated circuit.

37. (Original) The apparatus as recited in claim 36 wherein the resonating device is one of a crystal and a surface acoustic wave (SAW) device.

38. (Original) The apparatus as recited in claim 26 wherein a serial command sent to the input terminal is utilized to communicate to the apparatus that the calibration clock is going to be supplied.

39. (Original) The apparatus as recited in claim 36 wherein the package is a ceramic package.

40. (Original) The apparatus as recited in claim 33 wherein when the terminal is used as a serial data port, data transitions on the terminal occur at less than the predetermined interval and the data transitions do not change a current value of the internal output enable signal.

41. (Original) The apparatus as recited in claim 40 wherein the serial data port is bi-directional.

42. (Previously presented) An apparatus comprising:
a terminal for receiving a signal;
a resonating device supplying a reference signal having a fixed frequency;

a controllable oscillator coupled to receive the reference signal and generate a clock signal;

means for calibrating the apparatus utilizing a calibration clock supplied on the terminal by internally generating, in a phase-locked loop, one or more control values for the controllable oscillator to cause the oscillator to output a signal corresponding to the calibration clock; and

a non-volatile storage storing one or more values corresponding to the one or more control values.

43. (Original) The apparatus as recited in claim 42 wherein the apparatus comprises an integrated circuit and a resonating device in a sealed package.

44. (Previously presented) The apparatus as recited in claim 42 wherein the means for calibrating further generates at least a second control value using the phase-locked loop to lock the clock generated by the controllable oscillator to a multiple of the calibration clock and wherein the one control value and the second control value are generated at first and second temperatures.

45. (Previously presented) The apparatus as recited in claim 44 wherein the first and second temperatures are stored in the non-volatile storage.

46. (Previously presented) The apparatus as recited in claim 44 wherein a difference between the at least one control value at the first temperature and the second control value at the second temperature is stored in the non-volatile storage.

47. (Previously presented) The method as recited in claim 21 further comprising:

generating a second control value using the control loop to lock the clock generated by the controllable oscillator to a multiple of the calibration clock, wherein the control value and the second control value are generated at first and second temperatures; and

storing a second value associated with the second control value in the nonvolatile memory.

48. (Previously presented) A device including an integrated circuit calibrated according to the method of claim 47.